REMARKS

Claims 1-14 and 16-30 are pending. In a previous Office Action, the Examiner rejected claims 1-14 and 16-30 under were rejected under have been rejected under 35 U.S.C. 102(b) and 35 U.S.C. 103 as being unpatentable over Meizlik (6,112,323). The Examiner indicated that the arguments with respect to the pending claims in the Applicant's previous response were persuasive and the rejection has now been withdrawn. The Examiner is now entering a new grounds for rejection of the claims. Claims 1-14 and 16-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Normoyle (USP 5,892,957).

Normoyle describes an interrupt scheme. "The randomness of the period of time that the master waits before resending an INT request helps to prevent situations where a given interrupter repeatedly sends interrupts to another device, preventing the receiving device from sending its own interrupts (by causing it to delay its own interrupts to process incoming interrupts from the first interrupter). (In this application, "random" may be taken to mean either truly random or pseudorandom, i.e. random with certain predetermined constraints.) Thus, the interrupter is caused to delay some random period of time, and in that period the second device gets a chance to clear the outstanding interrupt(s) and issue its own interrupt request. This promotes evenhandedness in the ability of each master to deliver interrupts." (column 22, lines 47-60).

Normoyle does describe randomness of a period of time that the master waits before resending an INT request. However, Normoyle does not teach or suggest any delay introduced by a secondary or slave component. Furthermore, Normoyle does not teach or suggest any delay introduced by a secondary or slave component when responding to a primary component request. For example, Normoyle describes "the randomness of the period of time that the master waits before resending an INT request helps to prevent situations where a given interrupt repeatedly sends interrupts to another device." (column 22, lines 47-50) Normoyle also describes a primary component delaying an interrupt to another primary component. "Hence the delayed retry of the interrupt transaction by the interrupter, especially when it is a processor generating the interrupt to another processor, does not violate any processor memory models." (Summary) Sometimes a master component delays processing of a request from a slave component, but this type of delay is different from the typical Normoyle delay as it is not pseudo random. Plus this delay is still master component delay. "Some such possible constraints relate to delaying the

processing of a memory or slave request by a given master until any requests to any other memory or slave, respectively, by that same master are resolved." (Figure 3A Description) Normoyle is not believed to describe any slave or secondary component pseudo randomly delaying a response to a primary component.

By contrast, independent claim 13 recites "a delay mechanism configured to determine values operable to delay responses to requests received through the interconnection module, wherein the values are pseudo-randomly generated values." Independent claim 21 explicitly recites "wherein the plurality of secondary components are configured to determine delay values for adjusting response times to requests received through arbitration logic, wherein the values are pseudo-randomly generated values." Independent claims 1 and 28 recite "means for receiving a request at a secondary component coupled to a primary component through arbitration logic, the request characteristic of a primary component request" and "pseudo-randomly delaying a response to the request."

Normoyle is believed to describe only primary component pseudo randomly delaying interrupts or non-pseudo randomly delaying responses. The Examiner may attempt to argue that it would be obvious to also apply this to secondary components. The Applicants respectfully disagree. Normoyle pseudo randomly delays primary component interrupts to "prevent situations where a given interrupter repeatedly sends interrupts to another device, preventing the receiving device from sending its own interrupts." (column 22, lines 47-50) The claims are reciting responses to a primary component, so a secondary component would only respond upon receiving a request from a primary component. The motivation for pseudo randomly delaying secondary component responses lies in the ability to test an arbitration logic. For example, it may be useful to test whether arbitration logic fails if a secondary component waits an excessively long period of time to respond. Nowhere does Normoyle suggest any testing of any arbitration fabric or otherwise.

CONCLUSION

In light of the above remarks relating to the independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,

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